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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PAPE, ZACHARY	

ART UNIT	PAPER NUMBER
2835	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,223	LIN ET AL.	
	Examiner	Art Unit	
	Zachary M. Pape	2835	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/24/2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The following detailed action is in response to the correspondence filed 10/24/2005.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-7, 9, 11-22, 24, 26-29 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-4, 6-8, 14-19, 21-23, 27-29 of copending Application No. 10824090. Although the conflicting claims are not identical, they are not patentably distinct from each other because for the reasons detailed below.

3. With respect to claim 1, said claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 of copending application 10/824,090 (hereinafter referred to ass 090). With respect to claim 1, both the present application and the confliction application (090) recite, "a first circuit board including a first surface, with a grounding layer formed thereon, a second circuit board coupled to the first circuit board, including a second surface facing the first surface, wherein a second ground layer is formed on the second surface". The present application recites the use of "a plate-type heat dissipation device disposed between the first circuit board and the second circuit board, abutting the first ground layer and the second ground layer respectively" whereas the conflicting application states, "a heat dissipation fin disposed between the first circuit board and the second circuit board, abutting the first grounding layer and the second ground layer respectively". It would

have been obvious to one of ordinary skill in the art at the time the invention was made to replace the heat dissipation fin of (090) with a plate-type heat dissipation device since a plate-type heat dissipation device could include a heat dissipation fin.

With respect to claim 2 of the present application, said claim 2 recites, "the first circuit board further includes a third surface, opposite to the first surface, with a first device located thereon" whereas claim 2 of application 090 recites, "the first circuit board further includes a third surface, opposite to the first surface, with a first device located thereon".

With respect to claim 3 of the present application, said claim 3 recites, "the second circuit board further includes a fourth surface, opposite to the second surface, with a second device located thereon" whereas claim 3 of application 090 recites, "the second circuit board further includes a fourth surface, opposite to the second surface, with a second device located thereon".

With respect to claims 4-5 of the present application, said claims 4 and 5 of the state, "wherein the first ground layer comprises a copper layer" and "wherein the second layer comprises a copper layer", whereas claim 4 of application 090 states, "wherein the first ground layer and the second ground layer are made of copper".

With respect to claim 6 of the present application, said claim 6 recites, "further comprising a flat cable connecting the first circuit board and the second circuit board, providing communicability therebetween", whereas claim 6 of application 090 states, "further comprising a flat cable connecting the first circuit board and the second circuit board, providing communicability therebetween".

With respect to claim 7 of the present application, said claim 7 recites, "wherein the first circuit board includes a first connector, the second circuit board includes a second connector corresponding to the first connector, and the first circuit board and the second circuit board communicate with each other by the respective connectors" whereas claim 7 of application 090 states, "a connector connecting the first circuit board and the second circuit board, providing communicability therebetween". While claim 7 of 090 fails to teach that each of the circuit boards includes a connector, each circuit board must inherently comprise a connector for the other connector to connect to.

With respect to claim 9 of the present invention, said claim 9 recites, "a slot connector connecting the first circuit board and the second circuit board, providing communicability therebetween", whereas the combination of claims 1, 7, and 8 recite the limitations of claim 1 as well as, "a connector connecting the first circuit board and the second circuit board, providing communicability therebetween, wherein the connector is a slot connector".

With respect to claim 13 of the present invention, said claim 13 recites, "a first adhesion layer, disposed between the plate-type heat dissipation device and the first ground layer, for combining the plate-type heat dissipation device with the first circuit board; and a second adhesion layer, disposed between the plate-type heat dissipation device and the second ground layer, for combining the plate-type heat dissipation device with the second circuit board", whereas claim 13 of application 090 states, "a first adhesion layer, disposed between the plate-type heat dissipation device and the first ground layer, for combining the plate-type heat dissipation device with the first circuit

board; and a second adhesion layer, disposed between the plate-type heat dissipation device and the second ground layer, for combining the plate-type heat dissipation device with the second circuit board".

With respect to claim 14 of the present invention, said claim 14 recites, "both the first adhesion layer and the second adhesion layer comprise one selected from the group consisting of brazing solder, tin solder, thermal interface material, grease and the combination thereof respectively", whereas claim 13 of application 090 states, "both the first adhesion layer and the second adhesion layer comprise one selected from the group consisting of brazing solder, tin solder, thermal interface material, grease and the combination thereof respectively".

With respect to claim 15, both the present application and the confliction application (090) recite, "a first circuit board including a first surface, with a first heat conduction layer formed thereon, a second circuit board coupled to the first circuit board, including a second surface facing the first surface, on which a second heat conduction layer is formed". The present application further recites, "a plate-type heat dissipation device disposed between the first circuit board and the second circuit board, abutting the first heat conduction layer and the second heat conduction layer respectively" whereas conflicting application 090 states, "a heat dissipation fin disposed between the first circuit board and the second circuit board, abutting the first heat conduction layer and the second heat conduction layer". It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the heat

dissipation fin of (090) with a plate-type heat dissipation device since a plate-type heat dissipation device could include a heat dissipation fin.

With respect to claim 16 of the present invention, said claim 16 recites, "wherein the first heat conduction layer is a ground layer of the first circuit board, and the second heat conduction layer is a ground layer of the second circuit board", whereas claim 16 of application 090 states, "wherein the first heat conduction layer is a ground layer of the first circuit board, and the second heat conduction layer is a ground layer of the second circuit board".

With respect to claim 17 of the present invention, said claim 17 recites "the first circuit board further includes a third surface, opposite to the first surface, with a first device located thereon" whereas claim 17 of application 090 recites "the first circuit board further includes a third surface, opposite to the first surface, with a first device located thereon".

With respect to claim 18 of the present invention, said claim 18 recites, "the second circuit board further includes a fourth surface, opposite to the second surface, with a second device located thereon" whereas claim 18 of application 090 claim 18 recites, "the second circuit board further includes a fourth surface, opposite to the second surface, with a second device located thereon".

With respect to claim 19 of the present invention, said claim 19 recites, "the first heat conduction layer comprises a copper layer" whereas claim 19 of application 090 recites, "the first heat conduction layer comprises a copper layer".

With respect to claim 20 of the present invention, said claim 20 recites, "the second heat conduction layer comprises a copper layer" whereas claim 19 of application 090 recites, "the second heat conduction layer comprises a copper layer".

With respect to claim 21 of the present invention, said claim 21 recites, "a flat cable connecting the first circuit board and the second circuit board, providing communicability therebetween" whereas claim 21 of application 090 recites, "a flat cable connecting the first circuit board and the second circuit board, providing communicability therebetween".

With respect to claim 22 of the present invention, said claim 22 recites, "wherein the first circuit board includes a first connector, the second circuit board includes a second connector corresponding to the first connector, and the first circuit board and the second circuit board communicate with each other by the respective connectors" whereas claim 22 of application 090 recites, "a connector connecting the first circuit board and the second circuit board, providing communicability therebetween".

With respect to claim 24 of the present invention, said claim 24 recites, "a slot connector connecting the first circuit board and the second circuit board, providing communicability therebetween" whereas claims 22 and 23 of application 090 recite, "a connector connecting the first circuit board and the second circuit board, providing communicability therebetween, wherein the connector is a slot connector".

With respect to claim 28 of the present invention, said claim 28 recites, "a first adhesion layer, disposed between the plate-type heat dissipation device and the first heat conduction layer, attaching the plate-type heat dissipation device to the first circuit

board; and a second adhesion layer, disposed between the plate-type heat dissipation device and the second heat conduction layer, attaching the plate-type heat dissipation device to the second circuit board", whereas claim 27 of application 090 recites, "a first adhesion layer, disposed between the heat dissipation fin and the first heat conduction layer, attaching the heat dissipation fin to the first circuit board; and a second adhesion layer, disposed between the heat dissipation fin and the second heat conduction layer, attaching the heat dissipation fin to the second circuit board".

With respect to claim 29 of the present invention, said claim 29 recites, ""both the first adhesion layer and the second adhesion layer comprise one selected from the group consisting of brazing solder, tin solder, thermal interface material, grease and the combination thereof respectively", whereas claim 28 of application 090 states, "both the first adhesion layer and the second adhesion layer comprise one selected from the group consisting of brazing solder, tin solder, thermal interface material, grease and the combination thereof respectively".

4. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8, 11, 13, 14-23, 26, 28, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Collins et al. (US 5,218,516) in view of Nakamori (US 5,995,370).

With respect to claim 1, Collins et al. teaches a function module comprising: a first circuit board (32) including a first surface (See present office action Fig 1 below); a second circuit board (32) coupled to the first circuit board (36, 38), including a second surface (See present office action Fig 1 below) facing the first surface; a plate-type heat dissipation device (12), disposed between the first circuit board and the second circuit board (As illustrated in Collins Fig 6). Collins et al. fails to teach a first ground layer formed on a first surface, a second ground layer on a second surface, and that the plate-type heat dissipation device abuts the first and second grounding layer. Nakamori teaches the conventionality of placing first (9) and second (3) ground layers onto respective surfaces on a pair of circuit boards. It would have been obvious to one of ordinary skill in the cooling art at the time the invention was made to place the ground layers (9, 3) of Nakamori on the first and second surfaces of the circuit boards of Collins et al. to provide a heat sink for dissipating heat from the heat generating components on the circuit board and onto the plate-type heat dissipation device (Nakamori Column 3, Lines 64-67).

With respect to claim 15, Collins et al. teaches a function module comprising: a first circuit board (32) including a first surface (See present office action Fig 1 above); a second circuit board (32), coupled to the first circuit board (Via 36, 38), including a second surface (See present office action Fig 1 above) facing the first surface, a plate-

type heat dissipation device (12), disposed between the first circuit board and the second circuit board (As illustrated in Fig 6). Collins et al. fails to teach a first heat conduction layer formed on a first surface, a second heat conduction layer on a second surface, and that the plate-type heat dissipation device abuts the first and second grounding layer. Nakamori teaches the conventionality of placing first (9) and second (3) heat conduction layers onto respective surfaces on a pair of circuit boards. It would have been obvious to one of ordinary skill in the cooling art at the time the invention was made to place the heat conduction layers (9, 3) of Nakamori on the first and second surfaces of the circuit boards of Collins et al. to provide a heat sink for dissipating heat from the heat generating components on the circuit board and onto the plate-type heat dissipation device (Nakamori Column 3, Lines 64-67).

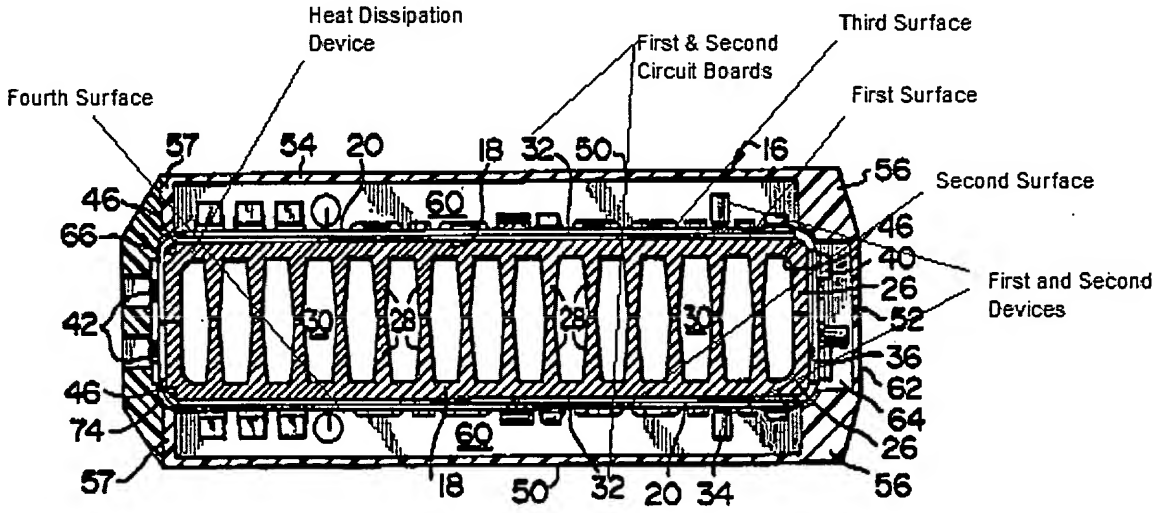

Fig 1

With respect to claims 2 and 17, Collins et al. further teaches that the first circuit board further includes a third surface (See present office action Fig 1 above), opposite the first surface, with a first device (34) located thereon.

With respect to claim 16, Nakamori further teaches that the first and second heat conduction layers is a ground layer (Column 3, Lines 18 and 26).

With respect to claims 3 and 18, Collins et al. further teaches that the second circuit board (32) further includes a fourth surface (See present office action Fig 1 above) opposite to the second surface, with a second device (34) located thereon.

With respect to claims 4, 5, 19, and 20 Nakamori further teaches that the first and second ground layers (3, 9) comprises a copper layer (Column 3, Lines 28-31).

With respect to claims 6 and 21, Collins et al. further teaches a flat cable (44) connecting the first circuit board and the second circuit board, providing communicability therebetween (Column 6, Line 65 – Column 7, Line 6).

With respect to claims 7 and 22, Collins et al. further teaches that the first circuit board (32) includes a first connector, the second circuit board (32) includes a second connector corresponding to the first connector, and the first circuit board and the second circuit board communicate with each other by the respective connectors (The flat cable (44) must inherently be connected to the circuit boards (32) via a connector on each in order to perform the function described in Column 6, Line 65 – Column 7, Line 6).

With respect to claims 8 and 23, Collins et al. further teaches that the first connector is located on the first surface, and the second connector is located on the second surface (As illustrated in Collins et al. Fig 2 where the part where 44 connects to

each respective circuit board is considered to be part of the first and second surfaces respectively).

With respect to claims 11 and 26, Collins et al. further teaches a heat dissipation fin (28), connected to the plate-type heat dissipation device, for further dissipation of heat therefrom (See Fig 6).

With respect to claims 13 and 28, Collins et al. further teaches a first adhesion layer, disposed between the plate-type heat dissipation device and the first ground layer, for combining the plate-type heat dissipation device with the first circuit board; and a second adhesion layer, disposed between the plate-type heat dissipation device and the second ground layer, for combining the plate-type heat dissipation device with the second circuit board (Column 7, Lines 13-16).

With respect to claims 14 and 29, Nakamori further teaches that both the first adhesion layer and the second adhesion layer comprise one selected from group consisting of brazing solder, solder, thermal interface material, grease and the combination thereof respectively (Column 7, Lines 13-16).

6. Claims 9 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Collins et al. in view of Nakamori and further in view of Harrison et al. (US 6,930,889).

With respect to claims 9 and 24, Collins et al. in view of Nakamori teach the limitations of claims 1 and 15 respectively but fail to teach a slot connector connecting the first circuit board and the second circuit board, providing communicability

therebetween. Harrison et al. teaches the conventionality of using a slot connector (50) for electrically and mechanically connecting one circuit board (1) to another circuit board (58). It would have been obvious to one of ordinary skill in the connector art at the time the invention was made to combine the slot connection teachings of Harrison et al. with the teachings of Collins et al. and Nakamori et al, to provide an alternate equivalent means of connecting two circuit boards together. Additionally, the slot connectors of Harrison et al. also reduce failure due to thermal damage (Harrison et al. Column 1, Lines 37-48, 61-62).

7. Claims 10 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Collins et al. in view of Nakamori and further in view of Juskey et al. (US 6,337,228).

With respect to claims 10 and 25, Collins et al. in view of Nakamori teaches the limitations of claim 1 and 15, but fails to teach that the plate-type heat dissipation device is a plate-type heat pipe, a copper plate, a plate-type copper block, a micro fin, a water-cooling device, or a vapor chamber. Juskey et al. teaches the conventionality of creating a heat dissipation device (20) out of copper (Column 5, Line 14). It would have been obvious to one of ordinary skill in the cooling art at the time the invention was made to combine the teachings of Juskey et al. with the teachings of Collins et al. and Nakamori such that the heat sink (12) of Collins et al. has good thermal conductivity (Juskey et al. Column 5, Lines 14-25).

8. Claims 12 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Collins et al. in view of Nakamori and further in view of DeHoff et al. (US 6,408,935).

With respect to claims 12 and 27, Collins et al. in view of Nakamori teaches the limitations of claim 11 above, but fails to teach that the function module further comprises a fan connected to the heat dissipation fin for further dissipation of heat therefrom. De Hoff et al. teaches the conventionality of attaching a fan (25) to a heat dissipation fin (23). It would have been obvious to one of ordinary skill in the cooling art at the time the invention was made to combine the fan of DeHoff et al. with the function modules of Collins et al. in view of Nakamori to provide enhanced cooling to the fins (DeHoff; Column 3, Lines 40-43). Enhancing the cooling of the fins reduces the heat buildup on the devices thus reducing malfunctions and breakdowns.

Response to Arguments

9. Applicant's arguments with respect to claims 1-11, 13-26, and 28-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zachary M. Pape whose telephone number is 571-272-2201. The examiner can normally be reached on Mon. - Thur. & every other Fri. (8:00am - 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynn Feild can be reached at 571-272-2092. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ZMP

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